L-Band 100-WATTs Push-Pull GaAs Power FET

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Abstract

Over 100W GaAs FET based device was developed. Using the push-pull configuration, this L-Band high power GaAs MESFETs achieved an output power of 102W(50.1dBm), 11.0dB power gain and 47% power added efficiency with drain-source voltage of 10V at 2.2GHz. In addition, operating with the drain-source voltage of 12V, an output power of 125W(51dBm) was obtained. The developed FET will contribute to improve the performance of the SSPAs used in various base-station systems that require higher output power and low distortion.

Introduction

Recently many kinds of communication systems like PCS and wireless local loop operating around 2GHz are widely developed. GaAs MESFETs have an advantage of high efficiency, better linearity and reliability compared to silicon devices. In order to use the FET chip for these high power application, it is necessary to combine the very low impedance FET chips, therefore push-pull configuration is better way to get the best FET chip performance. In this paper, the power performance of a newly developed L-Band over 100W Push-Pull GaAs power FET is reported. This output performance is about double compared with previous reported [1]. These MESFET chips utilize T-shaped Au gate technology for reliability and optimization of the breakdown voltage. The push-pull configuration was chosen for its frequency response and low distortion performance.

Fabrication Process and Chip Design

A cross section of the FET chip is shown in Figure 1. The key challenges are to reduce the source resistance and improve the gate-drain breakdown voltage (BVgdo). The recess structure reduces the source resistance and the gate-drain distance is optimized for higher gate-drain breakdown voltage. The source and drain ohmic contacts are formed by alloying Au/Ge/Ni/Au. The gate metal is WSi/Ti/Au.

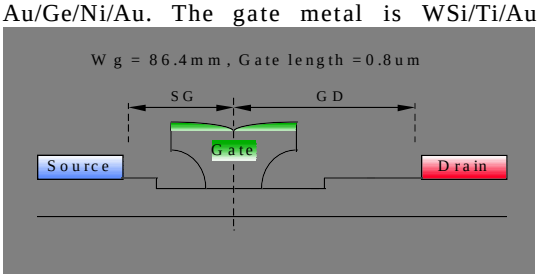

Fig.1 A cross section of the GaAs MESFET

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All active areas are covered with SiN passivation. The gate to source air-bridge crossover structure is used to reduce parasitic capacitance. The FET chip has a gold plated heat sink (PHS) and via-hole structure for reducing the thermal resistance and source inductance. The top view of the FET chip is shown in Figure 2. The gate length and the unit gate finger width of the chip are 0.8um and 600um, respectively. Total gate width is 86.4mm and the chip size is 1.1mm x 3.6mm.

Fig.2 Top view of FET chip (chip size = 1.1mm x 3.6mm)

FET PERFORMANCE

DC characteristics of the FET chip are shown in Figure 3. The typical saturated drain-source current (IDSS), drain-source conductance (gm), pinch-off voltage (Vp) and drain gate breakdown voltage (VGDO) are 12.5A, 8.8S, 1.8V and 29V respectively. The distributions of these parameters are very narrow. Figure 4 is an internal view of this push-pull FET. Four chips are assembled in the hermetic sealed package for reliability. The package is made of a metal base and metal wall. The metal wall was adopted based on the isolation and thermal analysis. Port to port isolation is better than -20dB. The base metal is optimized for thermal resistance. The typical thermal resistance of the overall device has been measured to be 0.8 degree C/W by the delta-VGS method. The four FET chips are combined in pairs within the package using lumped and distributed matching elements. Input and output port impedances are around 12 and 12 ohm input and output ports.

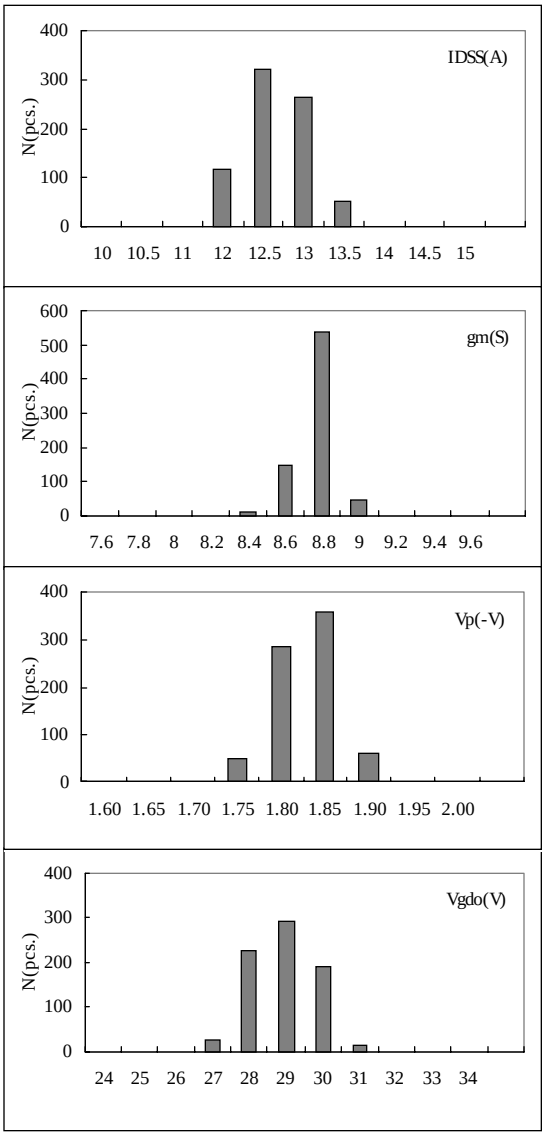

Fig.3 DC characteristics of chip.

The test fixture of the 100W push-pull FET is shown in Figure 5. This test fixture uses transmission lines and lumped capacitances for external input and output matching. First, the input and output port impedances are transformed to 25 ohms. Next, they are connected to baluns that transform the impedance to 50 ohms. The surface mount baluns are made by micro strip line. The balun size is only 7.2mm x 5.0mm with an insertion loss of 0.3dB [2]. The RF performance of the 100W Push-Pull FET is shown in Figure 6. Performance is measured with a drain-source voltage of 10V, 12V and a drain-source current of 6A (no RF). The FET achieved 102W output power with 11.0dB power gain and 47% power added efficiency at dorain-source voltage of 10V. When FET is tuned for optimized IMD, a third order inter-modulation distortion of -30dBc is achieved at an output power level of 45dBm (two tone) with class AB operation. The good third order inter-modulation was achieved by using push-pull technique. Since this FET has higher gate-drain breakdown voltage, this FET performed not only 102W output power at dorain-source voltage of 10V but 125W output power at dorain-source voltage of 12V with good correspondence of theoretical calculation.

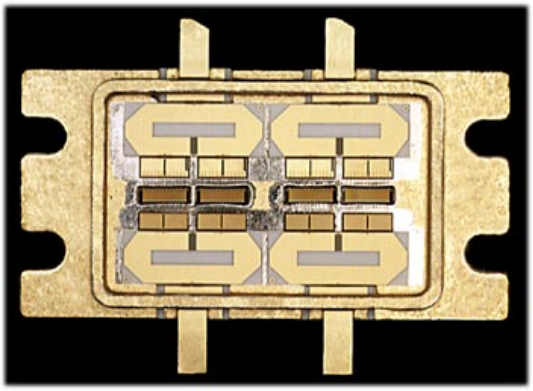

Fig.4 Internal view of 4-chip FET

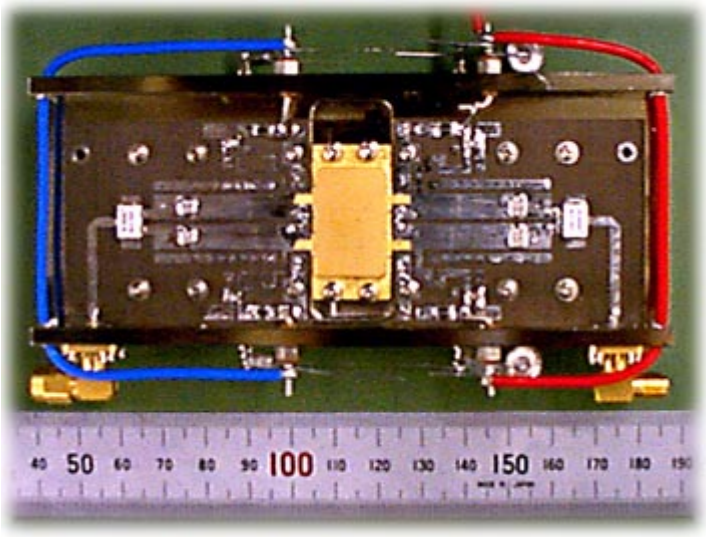

Fig.5 Test fixture drawing of the 100W push-pull FET

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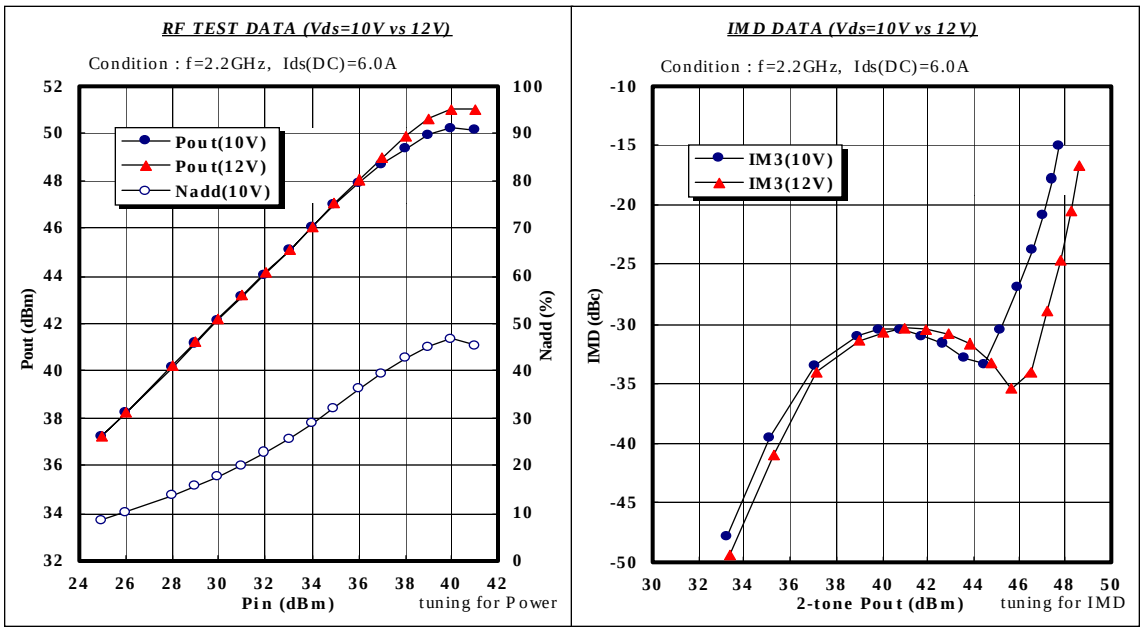

Fig.6 The RF performances of 100W Push-Pull FET

Conclusion

The 100W Push-Pull device has been developed. We achieved 102W output power with 11.0dB power gain and 47% power added efficiency at 2.2GHz with class AB operation. A third order inter-modulation distortion was achieved -30dBc at output power level of 45dBm (two-tone). In addition, operating with the drain-source voltage of 12V, an output power of 125W(51dBm) was obtained. The developed FET will improve base-station systems, which require higher power and low distortion.

Acknowledgment

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References

[1] G.Sarkissian, R.Basset, Z.Shingu and F.Ono. "A S-BAND PUSH-PULL 60-WATT GaAs MESFET FOR MMDS", IEEE MTT-S Digest, June 1997.

[2] SOSHIN ELECTRIC CO.LTD "BALUN DATA SHEET 1997"